JOHN L. GUSTAFSON

EDUCATION

B.S. (June 1977) in Applied Mathematics, with Honors
California Institute of Technology, Pasadena, California, P. G. Saffman, advisor
Applied Physics second major 1973–1976, J. R. Pierce, advisor

M.S. (June 1981) in Applied Mathematics
Iowa State University, Ames, Iowa
Thesis: "Total Positivity of Hypergeometric Functions," B. C. Carlson, advisor

Ph.D. (August 1982) in Applied Mathematics
Iowa State University, Ames, Iowa
Dissertation: "Asymptotic Expansions of Elliptic Integrals," B. C. Carlson, advisor

PROFESSIONAL EXPERIENCE

11/13 to present: **CTO, Ceranovo Inc.**

Responsible for overseeing all technical aspects of company, establishing Ceranovo's technical vision, directing its strategic direction, development, and future growth, provide leadership to department heads in a fashion that supports the company's culture, mission, and values, conduct research and case studies on leading edge technologies and make determinations of the probability of implementation; act as a good steward of the company's resources and ensure control of technology budgets.

6/13 to 11/13: **Consultant to MPT and author for CRC Press**

Assist Massively Parallel Technologies with the completion and productization of their collaborative cloud software development platform. Complete book on a new form of high-efficiency numerical computing for CRC Press, to be published March 2015.

8/12 to 6/13: **Senior Fellow, Chief Product Architect, AMD, Sunnyvale, CA**

Serve as technical lead for AMD's Graphics Processor Unit division. Evangelize AMD's graphics and high-performance computing approaches externally and internally; manage product road map; provide vision for future computing architectures to allow AMD to remain competitive.

3/09 to 8/12: **Director, Intel Corporation, Santa Clara, CA**

Directed an organization with about 50 researchers, mostly PhDs, working in a variety of areas. Funded and managed many university partners as well. The directorate was called XTL, for "eXtreme Technologies Lab," and was the part of Intel's research that is the most radical and visionary. The portfolio included energy-efficient computing and memory, for which we used FPGA-based emulators and software simulators as well as silicon prototyping; novel electrical energy storage approaches; free-space optics communications for consumer and data center applications; low-latency massively parallel computing operating systems; and new ways to represent real numbers for higher accuracy but lower bandwidth, energy, and storage requirements.

Directed Intel's participation in the $49 million DARPA Ubiquitous High Performance Computing (UHPC) program, which in a way is a successor to the DARPA HPCS program John directed at Sun Microsystems. Lab budget was around $30 million per year.

Filed about two patents per year, including two with over 40 sub-claims. Appointed to the Intel Patent Council that reviews the patent submissions from Intel employees. Awarded numerous awards within Intel for venturing efforts and solution of organizational problems.

3/09 to present: **Member, Board of Directors, Massively Parallel Technology Inc**. Position held concurrently with Director position at Intel and Senior Fellow position at AMD.

5/08 to 3/09: **Chief Executive Officer, Massively Parallel Technology Inc**. MPT is a privately held parallel computing company that was initially funded by the DARPA HPCS program (the same one that funded Cray, Sun, and IBM); it is now applying the patented IP it generated during that phase to the creation of firmware/hardware product lines that allow HPC clusters to scale to thousands of processors on a single problem. Its initial products will resemble network accelerators.

9/05 to 5/08: **Chief Technology Officer, ClearSpeed Technology Inc**. Responsible for technology of a 130-employee high-performance computing company with a 100^{+} million market capitalization. Identify and communicate present and future HPC requirements to company; serve as technical point of contact for strategic partners; identify gaps in current solution set and propose solutions; serve as spokesman to the HPC community; provide engineering with product guidance, wish lists, and help set priorities. Provide sales and marketing with analysis of algorithm-architecture fit. Develop and deliver demonstrations, prototypes, solutions, and proof-points. Create external technical papers and presentations. Create internal technical analyses for both executives and engineering.

9/04 to 9/05: **Principal Engineer, Sun Labs**. Application Architect for Sun's High-Performance Computing Systems (DARPA HPCS) program.

4/04 to 9/04: **Chief Technology Officer, ECS Inc**. Responsible for technology direction and portfolio for a startup computing integrator, Enterprise Cluster Solutions, Inc.

7/02 to 4/04: **Scientist, Sun Labs**. Responsible for defining High-Performance Computing (HPC) workloads for use in system measurement and analysis framework. Created novel benchmark approaches both for general Sun use and for Phase I of the DARPA High-Productivity Computing Systems (HPCS) program. Team lead for HPCS software as of 2/03; HPCS Principal Investigator as of 4/03 responsible for creation of Phase II proposal. Became Application Architecture Team Leader for HPCS Phase II.

3/00 to 7/02: **Senior Manager, Market Development Engineering, Sun Microsystems**. Responsible for engineering relationship between Sun and technical Independent Software Vendors (ISVs). Managed many direct reports and multiple interdepartmental projects involving benchmarking, porting, tuning, debugging, and scaling of ISV codes. Created and managed company-wide program for improving Sun product performance on the most commercially-significant ISV codes.

10/98 to 7/99: **Director of Ames Operations, Colorado MEDtech.** Responsible for developing software business unit for medical software engineering.

8/89 to 10/98: **Computational Scientist, Ames Laboratory.** Founder and Principal Investigator for the Scalable Computing Laboratory, performing research on advanced computer architectures, with attention to materials science, chemistry, physics, and graphics applications.

Adjunct Associate Professor, Iowa State University, Department of Computer Science, Department of Mathematics.

8/87 to 8/89: **Member of the Technical Staff, Sandia National Laboratories.** Developed applications for massively parallel computers and analyzed performance. Proposed and published new directions for high speed computing.

10/86 to 8/87: **Staff Scientist, nCUBE.** Analyzed hypercube computer architecture and application fit for scientific customers, engineers, and marketing/sales.

8/82 to 10/86: **Senior Staff Scientist** and **Product Development Manager, Floating Point Systems, Inc.** Directed development of ECL- and VLSI-based scientific computers for target markets; acted as liaison between Engineering and Marketing; managed group that planned and executed product introductions.

2/78 to 8/82: **Software Reliability Engineer, Jet Propulsion Laboratory** in Pasadena. Enforced top-down software development process for the Deep Space Net.

PATENTS

Method and apparatus for bezel mitigation with head tracking, filed June 18, 2014

Fabrication of porous silicon electrochemical capacitors, US 20140233152 A1

Integration of energy storage devices onto substrates for microelectronics and mobile devices, US20140226260 A1

High-efficiency illumination, WO2012040668 A3

Energy storage device, method of manufacturing same, and mobile electronic device containing same, US 20140078644 A1

Overcoming variance in stacked capacitors, US 20140036412 A1

Energy storage structure, method of manufacturing a support structure for same, and microelectronic assembly and system containing same, US 20130279137 A1

Rack to rack optical communication, US 20120155885 A1

Charge storage device, method of making same, method of making an electrically conductive structure for same, mobile electronic device using same, and microelectronic device containing same, CA 2794714 A1

Method of increasing an energy density and an achievable power output of an energy storage device, WO 2013048465

Method and apparatus for accuracy-aware analysis (7,448,026)

Precision improvement method for the Strassen/Winograd matrix multiplication method (7,209,939)

Method for tracking company-wide performance tuning projects (pending; US application 10292850)

Method for simultaneous overlapped communications between neighboring processors (5,072,371)

Method and system for benchmarking computers (scalable benchmarking) (5,245,638)

Methods for operating parallel computing systems employing sequenced communications (5,935,216)

HONORS AND AWARDS

2011 **Atanasoff Achievement Award**, Iowa State University
2007 Election to **IEEE Golden Core** (highest membership level)
2006 Inaugural **IEEE International Atanasoff Award**
2000 **Iowa State University Inventor of the Year Award**
1998 **Distinguished Visiting Professor, New Mexico State University**
1997 **PDPTA Outstanding Achievement Award**
1995 **R&D 100 Award**
1991 **R&D 100 Award**
1990 **New Mexico Inventor of the Year Award**
1989 **R&D 100 Award**
1988 Parallel computing breakthrough read into U.S. Congressional Record
1988 **Gordon Bell Award** (Greatest annual contribution to the science of parallel processing)
1988 **Karp Challenge** (First demonstration of parallel speedup of over 200 times)
1977 **Richter Fellowship**
1977 **Graduation with Honors, Election to Gnome Club** (Caltech honor society)
1974 **Eric Temple Bell Award** (Caltech; for “Outstanding Original Research in Mathematics”)
1973 **Drake Physics Prize**

MAJOR ACCOMPLISHMENTS

2013: Created new universal number ("unum") format for computation for superior answers with less storage and energy cost, eliminating rounding error, overflow, and underflow. Used it to solve long-standing mathematical challenges, such as bounded solutions for the *n*-body problem, lossless evaluation of polynomials, deterministic evaluation of the power function, and solution to "The Table-Maker's Dilemma" problem. Basis for book "The End of Error: Unum Computation" that has received accolades as being possibly the future of computing.

2012: Created and led a Technology Strategic Long-Range Plan (TSLRP) at Intel, selected from 198 entries, proposing a new direction for high-efficiency floating-point arithmetic. Obtained strong endorsement from Intel C-level executives, and the senior VPs of Intel Architecture and the Software and Systems Group.

2010: Created and led an initiative in novel silicon-based energy storage at Intel; received special funding from the CEO and CTO and presented to the Board of Directors in 2011. Basis for five patent applications to the US Patent Office in 2011, containing a total of 340 claims (almost one new claim per day).

2006: Doubled the speed of ClearSpeed's accelerator product by inventing a fundamental change to its microcode, restoring the company's competitive position pending its next chip generation.

2003: Created software approach for HPCS that resolved competing requirements of massive parallelism, high programmer productivity, and support for legacy environments; used persistent file concept in combination with novel benchmark approach to show feasibility of letting computer offload human burden of parallel programming. Invented and prototyped an accuracy-aware debugging environment (AADE) to increase productivity by automating numerical analysis and detecting causes of accuracy loss. Created successful HPCS Phase II proposal, with $47 million funding from DARPA for Sun's petascale computing R&D.

2002: Invented Purpose-Based Benchmark (PBB) approach, solving several long-standing problems in defining representative workloads for technical/scientific computing. PBBs were embraced by DARPA and required for all vendors in Phase II as the method of measuring productivity. Created reference implementation of first PBB.

2001–2002: Initiated, designed, and executed Sun's "Tunathon II" program for the improvement of commercial software application performance on Sun platforms through company-wide collaborations. Chaired the oversight committee, set performance rules, coordinated submissions with Legal and Marketing departments, and awarded Sun employee bonuses based on performance gains achieved and delivered to customers.

2000: Rebuilt the HPC/EDA Market Development Engineering group at Sun Microsystems, Inc., creating effective coverage of Sun's $3 billion market share.

1996–1998: Completed a working replica of the historic (1939–1942) Atanasoff-Berry Computer built at Iowa State College. Demonstrated it for a national audience, ending a long-standing debate over who had invented the first electronic digital computer. Created publicity material, including World Wide Web site.

1993–1995: Created first computer program (PHOTON) to solve the Kajiya Rendering Equation for global illumination; PHOTON scales to any desired precision and runs on any number of distributed-memory processors. Unlike most graphics rendering programs, PHOTON produces physically correct light intensities and is not restricted to particular surface types.

1991–95: Created first broad-spectrum computer benchmarks (SLALOM and HINT) capable of fair comparison despite different memory sizes, precisions, architectures, and languages. The network version of HINT, "NetPIPE," is still in widespread use for communication benchmarking and is part of many Linux distributions.

1989–92: Founded and grew the Scalable Computing Laboratory to $3 million annual budget within Ames Laboratory. Amassed collection of supercomputers from commercially healthy vendors that is a university resource for research and education.

1988: Attained 14x Cray X-MP speed on a production radar simulation program, using a 1024-processor system. Improved cost-performance over existing methods by over 100x.

1987: Obtained unprecedented speedup (1020x) on 1024-processor system, for practical scientific programs, resulting in widespread industry adoption of massively parallel computing approaches. Developed scaled speedup concepts (including an alternative to Amdahl's law that predicts only limited parallel speedup, now recognized as "Gustafson's law"). Extended ideas to vector-parallel architectures. Created a suite of techniques for achieving high parallel efficiency.

1985: Championed the FPS "Tesseract," a radically parallel vector computer. First to suggest that future supercomputer systems would be room-filling clusters of racked commodity systems with message-passing parallelism. Defined hardware specifications, program development software, application software, and position with respect to other FPS products. Created and executed product introduction plan, created collateral material, and supported first installations.

1985: Participated in algorithmic and hardware design of the FPS-164/MAX, a scientific computer tailored to the matrix-intensive computations of the structural analysis and computational chemistry marketplaces. Served primary role in pricing, press tours, sales force education, and software functional specifications for the product.

1985: Created the first "Level 3" version of the Basic Linear Algebra Subroutines (BLAS), now the basis of LAPACK, ATLAS, and the modern LINPACK benchmark. Showed Jack Dongarra how to make LINPACK scalable and flexible enough to benchmark massively parallel computers, enabling what we now know as the TOP500 list.

1985: Planned and executed the introduction of the FPS-264, the first ECL computer produced by Floating Point Systems. Assembled strategy for the construction of Class VII computer facilities using clusters of that computer, applied successfully to four sites including the NSF Supercomputer Center at Cornell.

1983: Developed automatic source code analyzer for finding high-level post-compilation errors in JPL programs. Increased speed and thoroughness of efforts to prove program correctness.

1982–1997: Created a software company, Parallel Solutions, that generated about $250,000 in revenue for a 375-routine math library (150,000 lines of hand-tuned assembly language), real-time commodity trading, symbolic algebra, 3-dimensional plotting, structural beam analysis, insurance underwriting, and blood lipoprotein analysis, either on contract or for commercial sale.

EDITORIAL/ CONFERENCE RESPONSIBILITIES

External Advisory Board, Iowa State University Computer Science Dept. and Software Engineering Dept., (2009 –)

Subcommittee Chairman for Performance Evaluation, *Supercomputing 2008*

Program Committee, *IPDPS 2007*

Steering Committee and Program Committee, International Atanasoff Symposium (2006)

Program Committee, *Supercomputing* conferences (1991, 1993, 1995, 1998, 2003, 2005)

Editorial Board, *International Journal on High Performance Computing and Networking*, (2004)

Program Committee, *PDPTA* (1998)

Program Committee, *International Parallel Processing Symposium* (1995, 1996, 1997)

Applications Chair, *International Parallel Processing Symposium* (1996)

Subject Area Editor, *Journal of Parallel and Distributed Computing* (1990 – 1998)

Editorial Board, *Parallel and Distributed Computer Practices* (1997 –)

Editorial Advisory Board, *Scientific Programming* (1994 –)

Judge, *R&D 100 Awards* (1992, 1993, 1994,1996, 1997)

Judge, *Mannheim SuParCup* Awards (1993, 1994, 1995)

Program Committee, *PERMEAN* (1995)

Program Committee, *Frontiers of Massively Parallel Computation* (1992)

Program Chair, *Fourth Conference on Hypercubes, Concurrent Computers, and Applications* (1989)

DEPARTMENT OF ENERGY AND DARPA GRANTS

Sun's Phase II participation in the DARPA HPCS program: **$47,000,000 over three years**, plus matching funds from Sun. Author of the proposal that moved Sun from last place (of IBM, Cray, HP, SGI, and Sun) to first place (tied with IBM) in the down-select from Phase I.

Funding of the Scalable Computing Laboratory ranged from **$1,000,000 to $3,000,000 per year**, 1989–1999, and was dependent on an annual proposal to the DOE for research and development to be performed and its approval.

"Parallelization Agent for Legacy Codes in Environmental Modeling," **$484,382** for 1996–1999. With Suraj Kothari (Computer Science) and Eugene Takle (Atmospheric Science). *Environmental Protection Agency*, #EPA/600/F-95/017.

"High Performance Morphological Filtering of Cirrus Emission from Infrared Images," **$90,000** for 1993–1996. With John Basart (Electrical Engineering), Philip Appleton (Physics/Astronomy), and Jeffrey Pedelty (NASA/Goddard Space Flight Center). *NASA*, NRA-92-OSSA-2

"A Massively Parallel Global Mesoscale Model with Improved Surface-Layer Coupling," with Eugene Takle, **$90,000** for 1993–1996, *NASA High Performance Computing & Communications Program*.

"Performance Evaluation: Massively Parallel Computers," **$1,459,000** for 1988–1990. Lead investigator, with Robert Benner, Gilbert Weigand, and Guylaine Pollock (Sandia National Laboratories). Supplemental Research Proposal to Scientific Computing Staff, *Office of Energy Research, USDOE*.

The MasPar MP-2 at the Scalable Computing Laboratory was funded through an agreement with the Center for Non-Destructive Evaluation. **$100,000**, 1992.

BOOKS

B2015.1 J. Gustafson, *The End of Error: Unum Computing*, Chapman & Hall/CRC Computational Science Series, ISBN 1482239868, 432 pages, available March 2015.

TECHNICAL REPORTS AND ON-LINE PUBLICATIONS

T2007.4 J. Gustafson, "A Study of Accelerator Options for Maximizing Cluster Performance," ClearSpeed white paper, August 2007.

T2007.3 J. Gustafson, "Algorithm Leadership," *HPCWire* contributed article, April 2007. Online at http://www.clearspeed.com/docs/resources/Gustafson-ISC2007.pdf

T2007.2 J. Gustafson, "Escaping the Shackles of 20th-Century Computing," ClearSpeed presentation at ISC2007, Dresden, Germany, April 2007. Online at http://www.hpcwire.com/hpc/1347145.html

T2007.1 J. Gustafson, "Latency, Bandwidth, and Accelerators," ClearSpeed white paper, February 2007. Online at http://www.clearspeed.com/docs/resources/LatencyBandwidthPaper.pdf

T2006.3 J. Gustafson, "Understanding the Different Acceleration Technologies," ClearSpeed white paper, presented at SC'06. Online at http://www.hpcwire.com/hpc/1091512.html

T2006.2 J. Gustafson, "The New Limits on High Performance Computing," *HPCWire* contributed article, http://www.hpcwire.com/hpc/705814.html

T2006.1 J. Gustafson and B. Greer (Intel), "ClearSpeed Advance: A Hardware Accelerator for the Intel Math Library," March 2006. Online at http://www.clearspeed.com/docs/resources/ClearSpeed_Intel_Whitepaper_Mar07.pdf

T2005.1 Tim Curns, Editor, "Sun's Gustafson on Envisioning HPC Roadmaps for the Future," Online interview at http://www.hpcwire.com/hpcwire/hpcwireWWW/05/0114/109060.html

T1996.1 Alan Beck, Managing Editor, "Developer Details Advantages of HINT Benchmark." Online interview at http://www.hpcwire.com/archives/8569.html

T1995.1 J. Gustafson and M. Wikstrom, "A New Paradigm for Computer Users," *Ames Laboratory Technical Report IS-5119, UC-32*, July 1995. Online at http://www.scl.ameslab.gov/Publications/Gus/NewParadigm/NewParadigm.html

T1994.1 J. Gustafson and Q. Snell, "HINT: A New Way to Measure Computer Performance," *Ames Laboratory Technical Report IS-5109, UC-405*, August 1994. Online at http://www.scl.ameslab.gov/Publications/Gus/HINT/HINTAcrobat.pdf

T1993.2 M. Carter and J. Gustafson, "An Improved Hierarchical Radiosity Method," *Ames Laboratory Technical Report IS-J 4881*, January 1993.

T1993.1 M. Carter and J. Gustafson, "The Symmetric Radiosity Formulation," *Ames Laboratory Technical Report IS-J 4880*, January 1993.

T1992.1 J. Gustafson and S. Aluru, "Massively Parallel Searching for Better Algorithms, or How to do a Cross Product with Five Multiplications," *Ames Laboratory Technical Report IS-5088, UC-32*, December 1992. Online at http://www.scl.ameslab.gov/Publications/Gus/FiveMultiplications/Five.html

T1991.3 M. Wikstrom, G. Prabhu, and J. Gustafson, "A Meta-Balancer for Dynamic Load Balancers," *Ames Laboratory Technical Report TR 91-04*, January 1991.

T1991.2 M. Wikstrom, G. Prabhu, and J. Gustafson, "The Work/Exchange Model," *Ames Laboratory Technical Report TR 91-03*, January 1991.

T1991.1 X. -H. Sun and J. Gustafson, "Toward a Better Parallel Performance Metric," *Ames Laboratory Technical Report IS-5049, UC-32*, January 1991.

T1990.1 J. Gustafson, D. Rover, S. Elbert, and M. Carter, "The Design of a Scalable, Fixed Time Computer Benchmark," *Ames Laboratory Technical Report IS-5049, UC-32*, April 1990.

T1988.2 J. Gustafson, "A Performance Model for Massive Parallelism," SAND ReportSAND88-1281, April 1988.

T1988.1 J. Gustafson, G. Montry, and R. Benner, "Development and Analysis of Scientific Application Programs on a 1024-Processor Hypercube," SAND Report, March 1988.

T1986.2 J. Gustafson, "Programming the FPS T Series," *Checkpoint*, June 1986.

T1986.1 J. Gustafson, "Parallel Processing using Multiple FPS Scientific Computers," *Checkpoint*, January 1986.

T1985.2 J. Gustafson, "First Electronic Digital Calculating Machine Forerunner to Cornell's FPS-164/MAX," *Forefronts*, Cornell University Theory Center publication, October 1985.

T1985.1 J. Gustafson, "The Measurement of Floating-Point Operations per Second," August 1985.

T1984.1 J. Gustafson, "A Comparison of the FPS-264 and FPS-164," *Checkpoint*, August 1984.

T1983.1 J. Gustafson, "Matrix Multiplication on the FPS-164," *Application Note*, Floating Point Systems, May 1983.

T1982.1 J. Gustafson and B. Greer, "Solving Tridiagonal Systems on the FPS-164," *Application Note*, Floating Point Systems publication, November 1982.

INVITED KEYNOTE LECTURES

(This section is incomplete. John gives about four keynote lectures per year, most of which are easily searchable on the web.)

K2007.5 "Predicting ClearSpeed Acceleration for Real Applications," Halmstead University (Sweden), May 31, 2007.

K2007.4 "Computing by the Liter," *HPC Asia*, Seoul, Korea, September 10, 2007.

K2007.3 "64-Bit Floating-Point Accelerators for HPC Applications," *Louisiana State University Computer Science Lecture Series*, September 5, 2007.

K2007.2 "Requirements for Successful Use of Accelerators," *Bay Area Beowulf Users Group (BayBUG)*, February 20, 2007.

K2007.1 "Acceleration Technologies: Fit for Purpose," *Hybrid Computing Conference*, Salt Lake City UT, January 31, 2007.

K2006.1 "The Quest for Linear Solvers and the Invention of Electronic Digital Computing," *JVA 2006 International Symposium on Computing*, Sofia, Bulgaria, October 2006.

K2004.2 "The Speed of Light Isn't What It Used to Be," *Tenth International Conference on Parallel and Distributed Systems (ICPADS 2004)*, July 2004.

K2004.1 "The New Parallel Processing Challenge: Watts," *Workshop on OpenMP Applications and Tools (WOMPAT)*, Houston, Texas, May 17, 2004.

K2003.1 "Sun's HPCS Approach: Hero," *Center for Advanced Scientific Computing (CASC) Conference*, Berkeley, California, August 7, 2003. Online at http://www.casc.org/meetings/CASC2.pdf

K2002.2 "Workload Benchmarks that Scale in Multiple Dimensions," *Fifth Workshop on Workload Characterization*, Austin, Texas, November 25, 2002.

K2002.1 "The Cost of the Single System Image," *International Conference on Parallel Processing*, Vancouver, British Columbia, August 2002.

K2000.1 "The Mainstreaming of Interval Arithmetic," *SCAN 2000*, Karlsruhe, Germany, September 2000.

K1999.1 "Conventional Benchmarks as a Sample of the Performance Spectrum," *Workshop on Performance Evaluation with Realistic Applications*, San Jose, CA, January 1999.

K1998.3 "Reconstruction of the Atanasoff-Berry Computer," *International Conference on the History of Computing*, Paderborn, Germany, August 1998.

K1998.2 "Making Computer Design a Science Instead of an Art," *HPCS '98*, Edmonton, Alberta, Canada, May 1998.

K1998.1 "Distributed Computer Performance Prediction," *National Center for Supercomputing Applications Seminar Series,* Champaign-Urbana, Illinois, April 1998.

K1997.3 "Cluster Computing," *Sixth IEEE International Symposium on High Performance Distributed Computing*, Portland, Oregon, August 1997.

K1997.2 "Forgotten Aspects of Computer Performance," *Parallel and Distributed Computing Techniques and Applications (PDPTA '97)*, Las Vegas, Nevada, July 1997.

K1997.1 "The Program of Grand Challenge Problems: Expectations and Results," *Second Aizu International Symposium on Parallel Algorithms/Architecture Synthesis*, Aizu-Wakamatsu, Japan, March 1997.

K1996.4 "Perspectives on Parallel Performance Metrics," *NATO Advanced Research Workshop in High Performance Computing: Technology & Applications*, Cetraro, Italy, June 24, 1996.

K1996.3 "Can We Make Software that Lasts Fifty Years?" *NATO Advanced Research Workshop in High Performance Computing: Technology & Applications*, Cetraro, Italy, June 25, 1996.

K1996.2 "A New Approach to Computer Performance Prediction," *Parallel Optimization Colloquium – POC '96*, Labortoire PRiSM, Université de Versailles, Versailles, France, March 1996.

K1996.1 "Difficulties in Measuring and Reporting Parallel Performance," *INFORMS CSTS Conference*, Dallas, Texas, January 1996.

K1995.3 "Broad-Spectrum Performance Analysis," *International Workshop on Computer Performance Measurement and Analysis (PERMEAN '95)*, Beppu, Japan, August 1995.

K1995.2 "Evaluating Parallel Computer Performance," *University of Iowa Computer Aided Engineering Network*, Iowa City, Iowa, May 1995.

K1995.1 "HINT: A New Way to Evaluate Computer Performance," *Caltech Symposium Series*, Pasadena, California, April 1995.

K1994.3 "Parallel Computer Performance Evaluation," *Michigan State University Lecture Series*, East Lansing, Michigan, October 1994.

K1994.2 "Experiences with the MasPar," *Parallel Processing Mini-Workshop*, Western University of London, Ontario, Canada, September 1994.

K1994.1 "A Paradigm for Grand Challenge Performance Evaluation," *Mardi Gras Conference on Teraflop Computing and Grand Challenge Applications*, Baton Rouge, Louisiana, February 1994.

K1993.2 "Evaluating Parallel Computer Performance," International Symposium in Mexico City, Mexico, November 1993.

K1993.1 "Parallel Performance Evaluation… And What the Vendors Won't Tell You," *Ford Motor Corporation Technical Symposium,* Dearborn, Michigan, March 1993. Also at MRJ Inc. Technical Symposium, McLean, Virginia, March 1992.

K1992.1 "The Consequences of Fixed-Time Performance Measurement," *Army High Performance Computing Research Center Colloquium Series*, Minneapolis, Minnesota, February 1992. Also at The Twenty-Sixth Hawaii International Conference on System Sciences, Kauai, Hawaii, January 1992.

K1991.3 "Parallel Performance Evaluation," Northern Illinois University, Seminar Series, DeKalb, Illinois, October 1991.

K1991.2 "Compute Intensive Applications On Advanced Computer Architectures," Queen Mary and Westfield College, University of London, London England, September 1991.

K1991.1 "Computing Research at Ames Laboratory," *Boeing Computer Services Presentation Series*, Huntsville, Alabama, June 1991.

K1990.2 "SLALOM: The First Scalable Computer Benchmark," Northern Illinois University, Seminar Series, DeKalb, Illinois, November 1990.

K1990.1 "Ray Tracing and Radiosity on Massively Parallel Computers," Ainu, Japan, August 1990.

K1988.1 "Parallel Applications on a 1024-Processor Hypercube," *Oregon Graduate Institute Lecture Series*, Beaverton, Oregon, April 1988.

REFEREED PUBLICATIONS

2006.1 J. Gustafson, "The Quest for Linear Solvers and the Invention of Electronic Digital Computing," *Proceedings of the JVA 2006 International Symposium on Computing*, Sofia, Bulgaria, October 2006, pp. 10–16.

2004.1 J. Gustafson, "Purpose Based Benchmarks," *International Journal of High Performance Computing Applications*, Volume 18, Issue 4 (November 2004), pp. 475–487.

2003.1 J. Gustafson, "Atanasoff-Berry Computer," entry in *Encyclopedia of Human-Computer Interaction*

2001.5 J. Gustafson, "John V. Atanasoff," *Encyclopedia of Computers and Computer History*, R. Rojas, Ed., Fitzroy Dearborn Publishers, 2001.

2001.4 J. Gustafson, "Hypercube Architecture," *Encyclopedia Computers and Computer History*, R. Rojas, Ed., Fitzroy Dearborn Publishers, 2001.

2001.3 J. Gustafson, "Cray-1," *Encyclopedia of Computers and Computer History*, R. Rojas, Ed., Fitzroy Dearborn Publishers, 2001.

2001.2 J. Gustafson, "Atanasoff-Berry Computer," *Encyclopedia of Computers and Computer History*, R. Rojas, Ed., Fitzroy Dearborn Publishers, 2001.

2001.1 J. Gustafson, "The Mainstreaming of Interval Arithmetic," chapter in *Perspectives on Enclosure Methods*, U. Kulisch, R. Lohner, A. Facius, eds., Springer-Verlag, 2001.

1999.1 J. Gustafson, D. Heller, R. Todi, and J. Hsieh, "Cluster Performance: SMP versus Uniprocessor Nodes," *Proceedings of Supercomputing '99*, (CD-ROM), ACM SIGARCH, November 1999.

1998.4 J. Gustafson, "Reconstruction of the Atanasoff-Berry Computer," *Annals of the History of Computing*, August 1998.

1998.3 J. Gustafson, "Making Computer Design a Science Instead of an Art, *Proceedings of the 12th Annual Canadian Conference on Computing Systems and Applications*, Edmonton, 1998.

1998.2 J. Gustafson, "Computational Verifiability of the ASCI Program," *IEEE Computational Science & Engineering*, March–June 1998.

1998.1 J. Gustafson and R. Todi, "Conventional Benchmarks as a Sample of the Performance Spectrum," *Proceedings of the Thirty-first Hawaii International Conference on System Sciences*, January 1998. Also in *The Journal of Supercomputing,* Volume 13, No. 3, May 1999, pp. 321–342.

1997.3 J. Gustafson "Distributed Means Clusters, Networks—and NT?" *IEEE Computational Science & Engineering*, July–September 1997.

1997.2 J. Gustafson, "The Program of Grand Challenge Problems: Expectations and Results," *Proceedings of the Second Aizu International Symposium on Parallel Algorithms/Architecture Synthesis*, pp. 2–7, Aizu-Wakamatsu, Fukushima, Japan. March 17–21, 1997.

1997.1 Q. Snell and J. Gustafson, "Parallel Hierarchical Global Illumination," *Proceedings of the Sixth IEEE International Symposium on High Performance Distributed Computing*, pp. 12–19, Portland, Oregon, August 5–8, 1997.

1996.5 Q. Snell and J. Gustafson, "An Analytical Model of the HINT Performance Metric," *Proceedings of Supercomputing '96*, Pittsburgh, Pennsylvania, IEEE Press, November 1996.

1996.4 J. Gustafson, "A New Approach to Computer Performance Prediction," *Proceedings of the Parallel Optimization Conference*, Versailles, France, March1996.

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